WHAT IS CLAIMED IS:

1. A horizontal sync detector, comprising:

a filter portion;

an equilibrium accumulator portion coupled to the filter portion;

a horizontal sync detector portion coupled to the filter portion and to the equilibrium accumulator portion; and

an output logic portion, coupled to the horizontal sync detector portion, the output logic portion adapted to produce a phase error based on a combined coarse phase error and a fine phase error.

2. The horizontal sync detector of claim 1, wherein the filter portion is adapted to output a flat filter to the equilibrium accumulator portion.

3. The horizontal sync detector of claim 2, wherein the equilibrium accumulator portion is adapted to determine at least one of a following level:

blank;

sync; and

trigger.

4. The horizontal sync detector of claim 3, wherein the at least one of the following levels are determined utilizing a floating equilibrium principle.

5. The horizontal sync detector of claim 3, wherein the equilibrium accumulator portion is adapted to determine a flat phase error based on the flat filter output and the trigger level.

6. The horizontal sync detector of claim 5, wherein the flat phase error is adapted to be received by the horizontal sync detector portion.

7. The horizontal sync detector of claim 6, wherein the horizontal sync detector portion is adapted to generate a level error.

8. The horizontal sync detector of claim 7, wherein the level error is a function of the flat phase error.

9. The horizontal sync detector of claim 6, wherein the horizontal sync detector portion is adapted to generate potential sync events.

10. The horizontal sync detector of claim 9, wherein the potential sync events are generated when the flat phase error crosses an adaptive trigger level.

11. The horizontal sync detector of claim 7, wherein the horizontal sync detector portion is adapted to generate a position error.

12. The horizontal sync detector of claim 11, wherein the horizontal sync detector portion is adapted to generate a total error.

13. The horizontal sync detector of claim 12, wherein the total error is equal to a sum of the level error and the position error.

14. The horizontal sync detector of claim 13, wherein a sync event occurs when the total error is smallest over a line.

15. The horizontal sync detector of claim 1, wherein the filter portion is adapted to output a Demmer phase error to the horizontal sync detector portion.

16. The horizontal sync detector of claim 15, wherein stable low jitter lock is achieved when the Demmer phase error is selected when clean noise free standard video input is detected.

17. The horizontal sync detector of claim 6, wherein a Demmer sync event occurs when a sub window is triggered by a zero crossing of the flat phase error .

18. The horizontal sync detector of claim 9, wherein the potential sync events are adapted to produce at least one of a following error at the output logic portion:

a coarse phase error; and

a fine phase error.

19. The horizontal sync detector of claim 18, wherein a phase error is produced at the output logic portion.

20. The horizontal sync detector of claim 19, wherein the phase error is equal to a sum of the coarse phase error and the fine phase error.

21. A method for determining phase error in a sync detector, the method comprising:

producing a flat phase error based on a flat filter output and on an equilibrium accumulator trigger level;

producing a level error based on the flat phase error;

producing a position error based on a modified pixel count;

producing a total error based on the position error and on the level error;

producing a coarse phase error based on the modified pixel count;

producing a fine phase error based on the level error and a previous level error; and

outputting a total phase error based on the fine phase error and the coarse phase error.

22. The method of claim 21, wherein the coarse phase error is equal to the modified pixel count.

23. The method of claim 22, wherein a pre-modified pixel count falls between 0 and pixels per line minus 1 (ppl-1).

24. The method of claim 23 further comprising modifying the pixel count to fall between –ppl/2 and ppl/2-1.

25. The method of claim 24 further comprising locking a horizontal phase-locked loop in a shortest time possible based on the modified pixel count between –ppl/2 and ppl/2-1.

26. The method of claim 25, wherein an absolute value of the modified pixel count is the position error.

27. The method of claim 21 further comprising producing the fine phase error by a divider.

28. The method of claim 27 further comprising generating an eight bit result which varies between -128 ... 0 ... +128 by the divider.

29. The method of claim 28 further comprising obtaining a perfect lock if the level error and the previous level error are centered about a trigger level such that a pixel count = an output pixel count =0.

30. The method of claim 29, wherein the modified pixel count is based on the pixel count.

31. The method of claim 29, wherein the trigger level is used to determine the flat phase error.

32. The method of claim 21 further comprising producing a valid sync event based on at least one of a following error from a list comprising:

the flat phase error; and

the total error.

33. The method of claim 32 further comprising updating buffer registers with a valid sync detected bit related to the valid sync event.

34. The method of claim 32 further comprising updating buffer registers with a valid sync detected bit for each valid sync event.

35. The method of claim 21 further comprising determining a difference between the flat filter output and the equilibrium accumulator trigger level to produce the flat phase error.

36. The method of claim 21 further comprising determining an absolute value of the modified pixel count to produce the position error.

37. The method of claim 21 further comprising adding the position error and the level error to produce the total error.

38. The method of claim 21 further comprising adding the fine phase error and the coarse phase error to produce the total phase error.

39. A method for determining phase error in a horizontal sync detector, the method comprising:

receiving pixels at a plurality of filters;

outputting a flat filter based on the filtered pixels to a plurality of accumulators;

outputting a trigger level by the plurality of accumulators based on the flat filter output;

producing a flat phase error based on the flat filter output and on the trigger level; and

producing a level error based on the flat phase error.

40. The method of claim 39 further comprising, if a count of the received pixels reaches an output pixel count, updating output registers with contents of a buffer register.

41. The method of claim 40 further comprising modifying the pixel count.

42. The method of claim 41 further comprising producing a position error based on the modified pixel count.

43. The method of claim 42 further comprising producing a total error based on the position error and on the level error.

44. The method of claim 43 further comprising initializing a stored total error to a maximum value.

45. The method of claim 44 further comprising, if the total error is less than the stored total error, indicating that a valid sync event has occurred.

46. The method of claim 45 further comprising updating buffer registers with a coarse phase error based on the modified pixel count; the level error; and a previous level error.

47. The method of claim 46 further comprising producing a fine phase error based on the level error and the previous level error.

48. The method of claim 46 further comprising outputting a total phase error based on the fine phase error and the coarse phase error.

49. A horizontal sync detector, comprising:

an input portion adapted to receive pixels; and

an output portion, coupled to the input portion, adapted to produce a phase error based on a combination of a coarse phase error and a fine phase error.